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EXAMINER	
KROFCHECK, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,480	ADL-TABATABAI ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,7-25,27-38,40-42,44,45 and 47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *35-38 and 40* is/are allowed.

6)☒ Claim(s) *1,3,5,7-11,13-21,23-25,27,30-33,41,42,44,45 and 47* is/are rejected.

7)☒ Claim(s) *5,8,9,12,22,28,29,34,41,44 and 45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/2/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on 1/9/2006.

2. The abstract has been amended.

3. Claims 2, 4, 6, 26, 39, 43, 46 have been cancelled.

4. Claims 1, 5, 8-11, 13, 23-25, 27, 29, 35-38, 40-42, 47 have been amended.

5. The rejections and objections not recited herein are withdrawn.

Information Disclosure Statement

6. US patent application publication 2003/217237 was not considered because it is an invalid published application.

Claim Objections

7. Claims 5, 7, 8, 9, 28, 29, 41, 44, 45 objected to because of the following informalities:

a. Relating to claims 5, 8, 9, the strikethrough of the reference to claim 4 is not visible, hence it should be replaced with double brackets around the deleted section.

b. Relating to claim 28, the second line contains the term, "ore" which should be "or".

c. Relating to claim 29, the strikethrough of the two deleted "e" is not clearly visible, hence it should be replaced with double brackets around the deleted section.

d. With respect to claim 41, the examiner noticed a slight discrepancy between the amended claim and the originally filed claim. The originally filed claim has 41 dependent on 37, but in the amended version, 41 is shown as initially being dependent on claim 26 (now cancelled) being changed to claim 24. Is this an error and claim 41 should still be dependent on claim 37?

e. Relating to claims 44 and 45, they are listed as "original", even though they have been amended to correct their dependency.

f. The claims not mentioned are objected to because of their dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claim 1, 3, 5, 7, 9-11, 14, 17-18, 21, 23-25, 27, 32-33, 41-42, 44-45, 47 rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger et al., U.S. Patent Application Publication 2003/0135694 and Auerbach et al., US patent 6199126.

11. With respect to claim 1, Naffziger teaches of a computer system comprising: a central processing unit (CPU) (fig. 1, item 103; paragraph 0040); and

a cache memory, coupled to the CPU (fig. 1, items 104 and 106; paragraph 0040), having a plurality of compressible cache lines to store additional data (fig. 2; paragraphs 0043-0044; where the cache is organized into cache lines made up of multiple sublines which decompress to full cache lines)

a cache controller to perform lookup operations of the cache memory (figs. 2, 3; items 240 and 330; paragraph 0062; The cache controller comprises the cache control, compression & decompression engines, and all other components that work together to control the 2nd level cache memory (items 210 and 310). The cache control has writeback, read-ahead, and eviction control logic)

the cache controller having an array of tag entries corresponding to each of the plurality of cache lines (fig. 3, 4; paragraph 0057-0059; where the address tag indicates where in the cache line group is the cache line associated with the address tag),

each tag entry having address tag bits corresponding to a cache line address (fig. 2, 3, 4; paragraph 0043, 0057-0059; where the address tag indicates where in the cache line group is the cache line associated with the address tag), and

one or more compression encoding bits indicating whether a corresponding cache line is compressed (fig. 3, 4; paragraph 0057-0059, 0061; the address tag is

associated with a compressed flag. The compressed flag indicates if the cache line is compressed).

one or more companion encoding bits indicating which companion lines are stored in a common cache set (figs. 3-4; paragraphs 0059; where the way indicator (companion encoding bits) associated with each address tag indicates where in the cache line group (cache set) the cache line associated with the address tag is stored).

Naffziger fails to explicitly teach of if the compression bit indicates the cache line is compressed the companion bit is treated as a part of an offset and if the compression bit indicates the cache line is not compressed the companion bit is considered a component of the address tag bits.

However, Auerbach teaches of if the cache line is compressed the companion bit is treated as a part of an offset and if the cache line is not compressed the companion bit is considered a component of the address tag bits (fig. 9; column 8, line 66-column 9, line 42; when uncompressed the offset (companion bits), is 0, thus the address is offset by 0 to reach the desired location).

Naffziger and Auerbach are analogous arts as they are both in the same field of endeavor, data compression in a memory. It would have been obvious to one of ordinary skill in the art having the teachings of Naffziger and Auerbach at the time of the invention to implement the index table containing the index offset format in the tag memory of Naffziger as taught in Auerbach. Their motivation would have been to enable the location of the second block of code, whether compressed or uncompressed (Auerbach, column 9, lines 3-10).

12. With respect to claim 23, the combination of Naffziger and Auerbach teaches of the limitations cited with respect to claim 1. Additionally, Naffziger teaches of a cache controller comprising: compression logic to compress lines within a cache memory device (figs. 2, 3; items 230, 308; paragraph 0051; where the compression engine compresses cache lines and sublines that contain partially uncompressed data into sublines).

13. With respect to claim 42, the combination of Naffziger and Auerbach teaches of the limitations cited with respect to claim 1. Additionally, Naffziger teaches of a computer system comprising: a central processing unit (CPU) (fig. 1, item 103; paragraph 0040);

a cache memory, coupled to the CPU (fig. 1, items 104 and 106; paragraph 0040), having a plurality of compressible cache lines to store additional data (fig. 2; paragraph 0043-0044; where the cache is organized into cache lines made up of multiple sublines which decompress to full cache lines);

a chipset coupled to the CPU (fig. 1, items 103 and 110; paragraph 0040; the system controller and the processor integrated circuit makeup a chipset); and

a main memory (fig. 1, item 110; paragraph 0040).

14. With respect to claims 3 and 44, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the cache controller is included within the CPU (figs. 2, 3; paragraph 0041; where the cache controller is included in the second level cache, which is located on the processor integrated circuit).

15. With respect to claim 24, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of set and way logic to select a plurality cache lines (figs. 2-4; paragraph 0056-0059; where the tag address (set) is used to find a corresponding tag line and the way indicator indicates where a cache line associated with the address tag is stored. Since the memory is addressable via address tags (sets) and ways, it is inherent that there is logic that selects the cache lines by this format).

16. With respect to claims 5, 25, and 47, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein a single cache line stores two or more cache lines if the corresponding compression bit indicates that the line is compressed (fig. 4-3; paragraphs 0043, 0059-0060 and 0066; where the cache line group (single cache line) stores multiple compressed cache lines, i.e. sublines. When stored in compressed form, the remaining space in the group is usable by other groups associated with the excess address tags).

17. With respect to claim 7, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the companion lines are adjacent memory lines (figs. 3-4; paragraphs 0059; where the data lines (companion lines) associated with the way indicators 0-15 are adjacent to each other).

18. With respect to claim 9, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of

wherein the companion encoding bits used to encode the ordering of companion lines in the compressed line (figs. 3-4; paragraphs 0059-0060; where the way indicator (companion encoding bits) associated with each address tag indicates where in the cache line group (cache line) the cache line associated with the address tag is stored. The cache line group is compressed in the cache data memory).

19. With respect to claim 10, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the cache controller further comprises set and way selection logic to select a cache line (figs. 2-4; paragraph 0056-0059; where the tag address (set) is used to find a corresponding tag line and the way indicator indicates where a cache line associated with the address tag is stored. Since the memory is addressable via address tags (sets) and ways, it is inherent that there is logic that selects the cache lines by this format).

20. With respect to claims 11 and 27, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the set and way selection logic comprises tag comparison logic to compare the cache line address to the address tag bits (figs. 2, 3; items 206, 320; paragraphs 0042 and 0062; where the tag comparator and hit logic compares the address field with the address tags).

21. With respect to claim 14, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the cache controller further comprises compression logic to compress a cache

line (figs. 2, 3; items 230, 308; paragraph 0051; where the compression engine compresses cache lines).

22. With respect to claim 17, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the compression logic determines when a cache line is to be compressed (fig. 3, paragraph 0060; where the compression engine determines if a cache line group is compressible and compresses it if it is).

23. With respect to claim 18, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the compression logic compresses a cache line based upon opportunistic compression (fig. 3; paragraph 0060; where the compression engine compresses the cache line group (cache line of compressed sublines) if it contains uncompressed data and is compressible).

24. With respect to claims 21 and 33, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the cache controller further comprises byte selection logic to select addressed datum within a cache line (fig. 2; paragraph 0044; a first data line pointer from the tag memory is used to locate the first subline, the first subline is located within the cache line of compressed sublines, of the referenced information in the cache data memory. As the pointer is used to locate this subline, there must be logic that connects the pointer to the desired location).

25. With respect to claim 32, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the compression logic determines when a cache line is to be compressed (fig. 3, paragraph 0060; where the compression engine determines if a cache line group is compressible and compresses it if it is).

26. With respect to claim 41, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of using the one or more companion encoding bits to encode the ordering of companion lines in the first cache line if the first cache line is compressed (figs. 3-4; paragraphs 0059-0060; where the way indicator (companion encoding bits) associated with each address tag indicates where (the order) in the cache line group (cache line) the cache line associated with the address tag is stored. The cache line group is compressed in the cache data memory).

27. With respect to claim 45, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of wherein the cache controller is included within the chipset (figs. 1-3; paragraph 0040-0041; where the cache controller is included in the second level cache, which is located on the processor integrated circuit, part of the chipset).

28. Claims 15-16, 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger and Auerbach.

29. With respect to claims 15 and 16, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also

teaches of using various compression algorithms to compress cache lines (fig. 3; paragraph 0064). Naffziger fails to explicitly teach of using a dictionary based or sign-bit compression algorithm.

The applicant states in paragraph 48, "In one embodiment, cache lines are compressed according to a Lempel-Ziv compression algorithm. However in other embodiments, other compression algorithms (e.g., WK, X-Match, sign-bit compression, run-length compression, etc.) may be used to compress cache lines."

It would have been obvious to one of ordinary skill in the art to use a dictionary based or a sign-bit compression algorithm to compress cache lines. One would have been motivated to use a dictionary based compression algorithm as they are commonly used in computers (such as the .gif and .zip formats), thus it would be compatible with numerous systems. One would have been motivated to use a sign-bit compression to compress cache lines as it would help to reduce the energy used to operate the cache memory.

30. With respect to claims 30-31, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger also teaches of using various compression algorithms to compress cache lines (fig. 3; paragraph 0064). Naffziger fails to explicitly teach of using a dictionary based or sign-bit compression algorithm.

The applicant states in paragraph 48, "In one embodiment, cache lines are compressed according to a Lempel-Ziv compression algorithm. However in other

embodiments, other compression algorithms (e.g., WK, X-Match, sign-bit compression, run-length compression, etc.) may be used to compress cache lines."

It would have been obvious to one of ordinary skill in the art to use a dictionary based or a sign-bit compression algorithm to compress cache lines. One would have been motivated to use a dictionary based compression algorithm as they are commonly used in computers (such as the .gif and .zip formats), thus it would be compatible with numerous systems. One would have been motivated to use a sign-bit compression to compress cache lines as it would help to reduce the energy used to operate the cache memory.

31. Claim 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger and Auerbach and Yanai et al., U.S. Patent 5,206,939 (hereinafter Yanai).

32. With respect to claim 8, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger fails to specifically teach of wherein the companion encoding bits used as a compression format bit to select between different compression algorithms. However, Yanai teaches of compression format bits to select between different compression algorithms (table 3; column 7, lines 55-57; where bits 0-3 indicate the compression algorithm).

The combination of Naffziger and Auerbach and Yanai are analogous arts as they both are related to data compression. It would have been obvious to one of ordinary skill in the art having the teachings of Naffziger, Auerbach and Yanai at the time of the invention to incorporate the compression algorithm selection bits from Yanai into the way indicator in the combination of Naffziger and Auerbach in order to allow the

different compression algorithms indicated in the combination of Naffziger and Auerbach to be indicated based on the way bits thus saving space in the cache memory and increasing the speed at which the data can be retrieved and decompressed.

33. Claims 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger and Auerbach and Gross, U.S. Patent Application Publication 2004/0255209 (hereinafter Gross).

34. With respect to claim 13, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger teaches of comparing a high order address field with address tags (paragraph 0062), but fails to specifically teach of wherein the tag comparison logic compares the one or more companion bits within the address with the one or more companion encoding bits within the tag if the compression encoding bits indicate that the cache line is not compressed.

However, Gross teaches of tag comparison logic compares the one or more companion bits within the address with the one or more companion encoding bits within the tag if the compression encoding bits indicate that the cache line is not compressed (fig. 2; paragraph 0021, where the high address part (companion bits) is compared by comparators (comparison logic) against the way addresses (companion encoding bits) to determine if the address has stored a hit in the cache. Cache hits are determined if a cache line is compressed or uncompressed. Therefore, they occur when the cache line is uncompressed).

The combination of Naffziger and Auerbach and Gross are analogous arts as they are both in the same field of endeavor, data compression in a cache memory. It

would have been obvious to one of ordinary skill in the art having the teachings of Naffziger and Auerbach and Gross at the time of the invention to include the logic that compares the high address part in with the way addresses located in the tag address in Gross into the tag compare logic in the combination of Naffziger and Auerbach. The motivation for this would have been to more accurately determine cache hits by comparing more of the addresses.

35. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger, Auerbach, and Wang et al., U.S. Patent 6,507,895 (hereinafter Wang).

36. With respect to claim 19, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger teaches of compression logic (figs. 2-3, items 230 and 308), but fails to specifically teach of compresses a cache line based upon prefetch compression

However, Wang teaches of compresses a cache line based upon prefetch compression (column 6, lines 14 – 20; where prefetch data can be compressed and stored in a compression cache).

The combination of Naffziger and Auerbach and Wang are analogous arts as they both involve data compression in a cache. It would have been obvious to one of ordinary skill in the art having the teachings of Naffziger, Auerbach and Wang at the time of the invention to modify the compression engine and control logic in the combination of Naffziger and Auerbach to compress prefetched data as is done in Wang. The motivation for this would have been to provide faster access (Wang, column 6, lines 14 – 20).

37. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger, Auerbach, and Shimoi et al., U.S. Patent 5,652,857 (hereinafter Shimoi).

38. With respect to claim 20, the combination of Naffziger and Auerbach teaches of all the limitations of the parent claims as discussed supra. Naffziger teaches of compression logic (figs. 2-3, items 230 and 308), but fails to specifically teach of compresses a cache line based upon victim compression.

However, Shimoi teaches of compresses a cache line based upon victim compression (fig. 7, column 10, line 61-column 11, line 12; where the uncompressed data in the cache memory is swept out buy the LRU and the compressing circuit compressed the data and stores it in the compression cache memory).

The combination of Naffziger and Auerbach and Shimoi are analogous arts as they both involve data compression in a cache. It would have been obvious to one of ordinary skill in the art having the teachings of Naffziger, Auerbach, and Shimoi at the time of the invention to modify the compression engine and control logic in the combination of Naffziger and Auerbach to compress data evicted from the L1 cache and store it in the L2 cache as taught in Shimoi. The motivation for this would have been to improve the capacity while limiting the costs of the system, Shimoi column 1, lines 21 - 23.

Allowable Subject Matter

39. Claims 35-38 and 40 are allowed.

40. Claims 12, 22, 28-29, 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

41. Applicant's arguments filed 1/9/2006 have been fully considered but they are not persuasive.

42. Applicant's arguments with respect to claims 1, 3, 5, 7-23, 42 have been considered but are moot in view of the new ground(s) of rejection.

43. Applicant's arguments with respect to claims 35, 38, 40 have been considered but are moot as independent claim 35 differs in scope from the other independent claims as argued. As the applicant has amended claim 35 to include the subject matter of previous claims 37-39, with the subject matter of previous claim 39 being allowable, claim 35 and its dependent claims are allowed.

Conclusion

44. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

45. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

46. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

47. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

48. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

49. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck

MATTHEW D. ANDERSON
PRIMARY EXAMINER